

Philips Semiconductors – a worldwide company

Contact information

For additional information please visit <http://www.semiconductors.philips.com>. Fax: **+31 40 27 24825**

For sales offices addresses send e-mail to: sales.addresses@www.semiconductors.philips.com.

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Quad 2-input AND gate

74HC08; 74HCT08

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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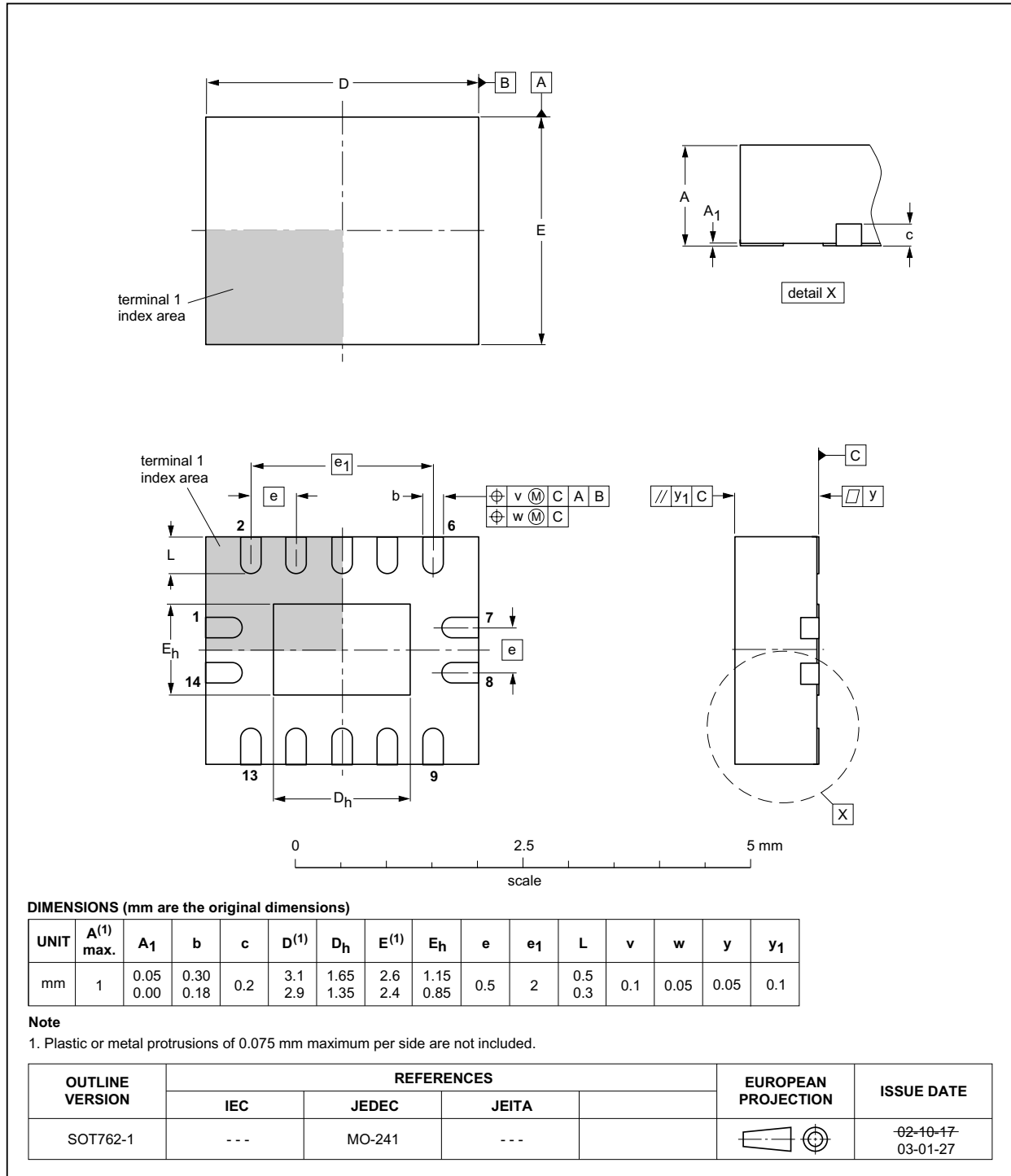
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Quad 2-input AND gate

74HC08; 74HCT08

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

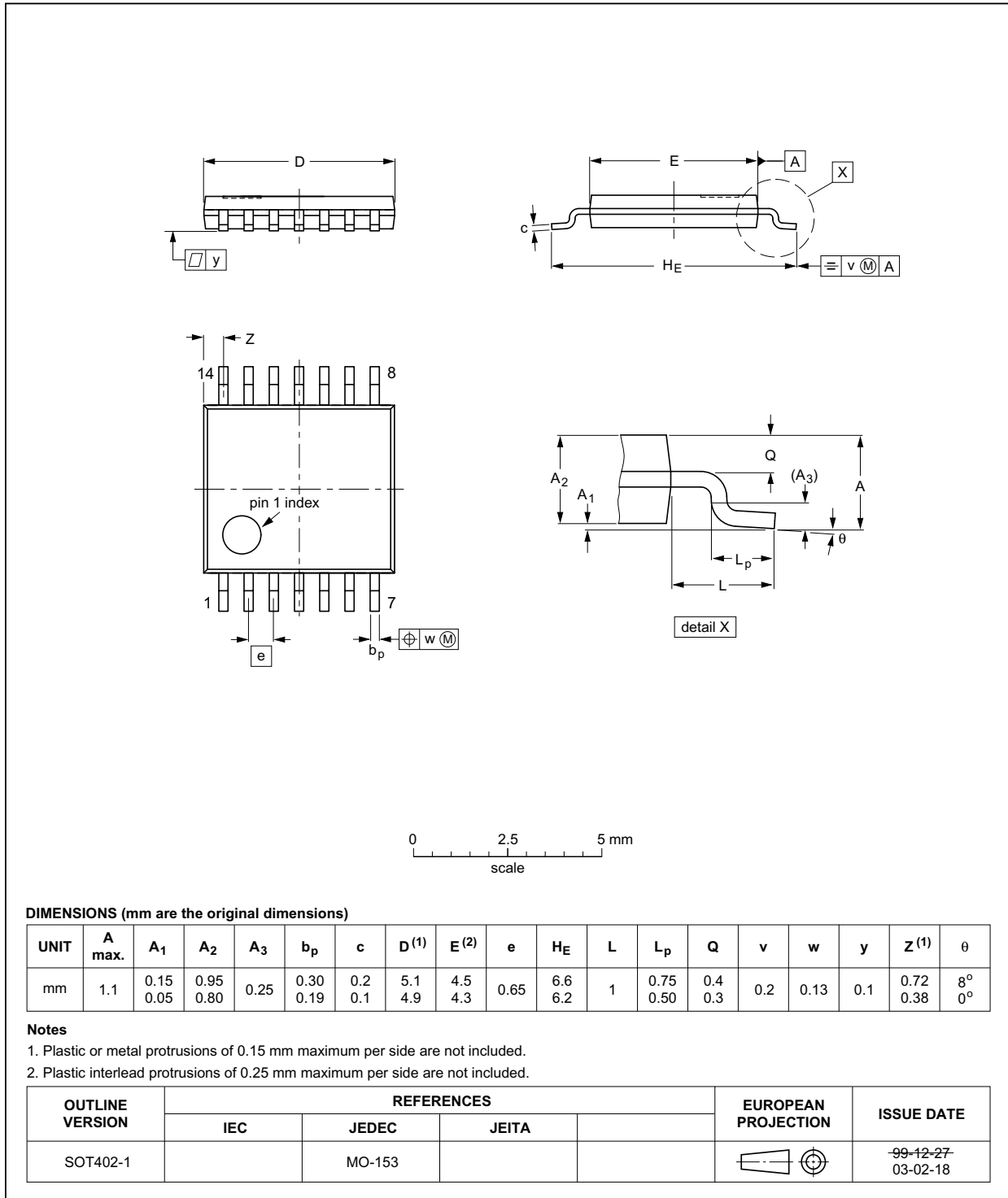


Quad 2-input AND gate

74HC08; 74HCT08

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

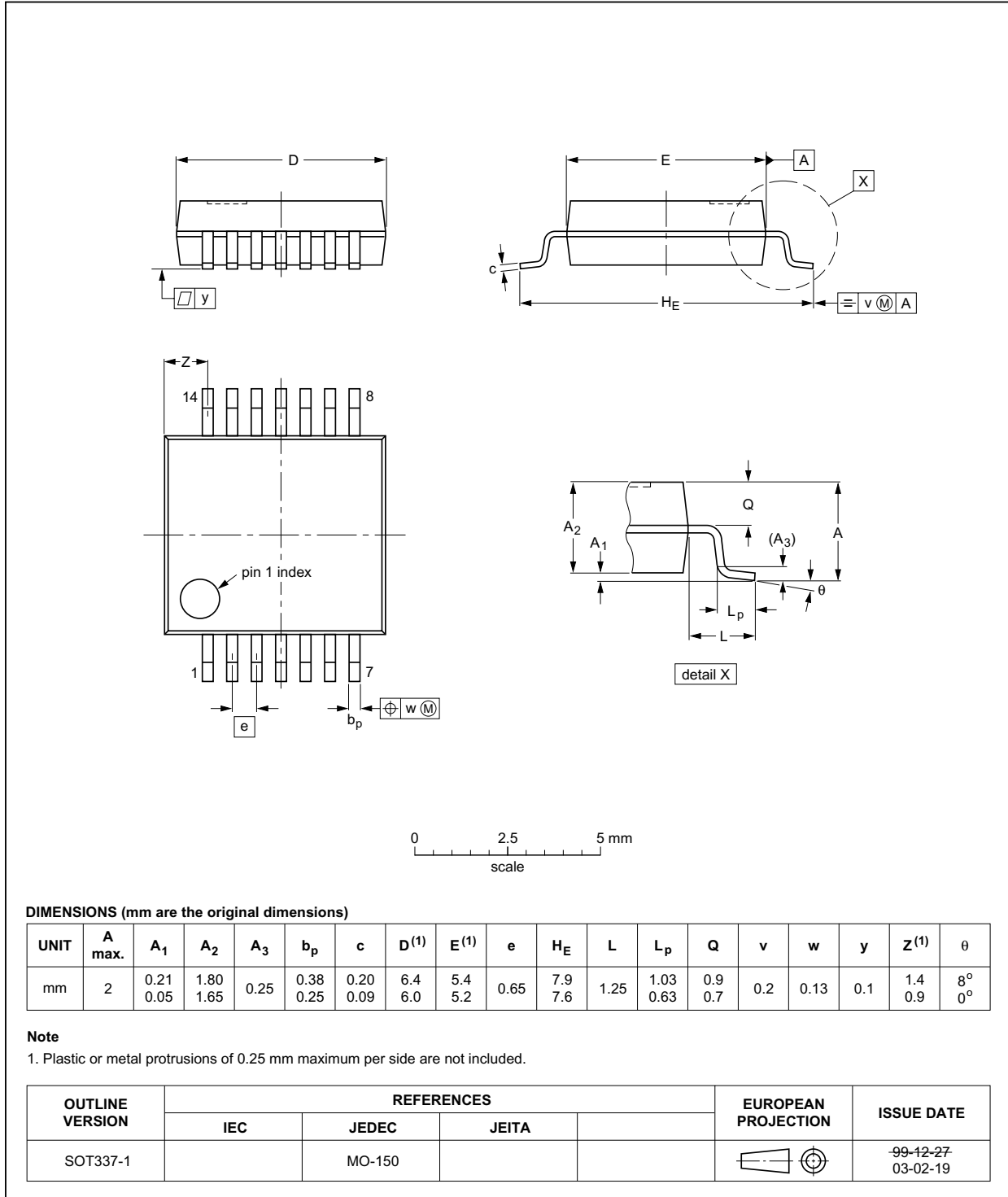


Quad 2-input AND gate

74HC08; 74HCT08

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

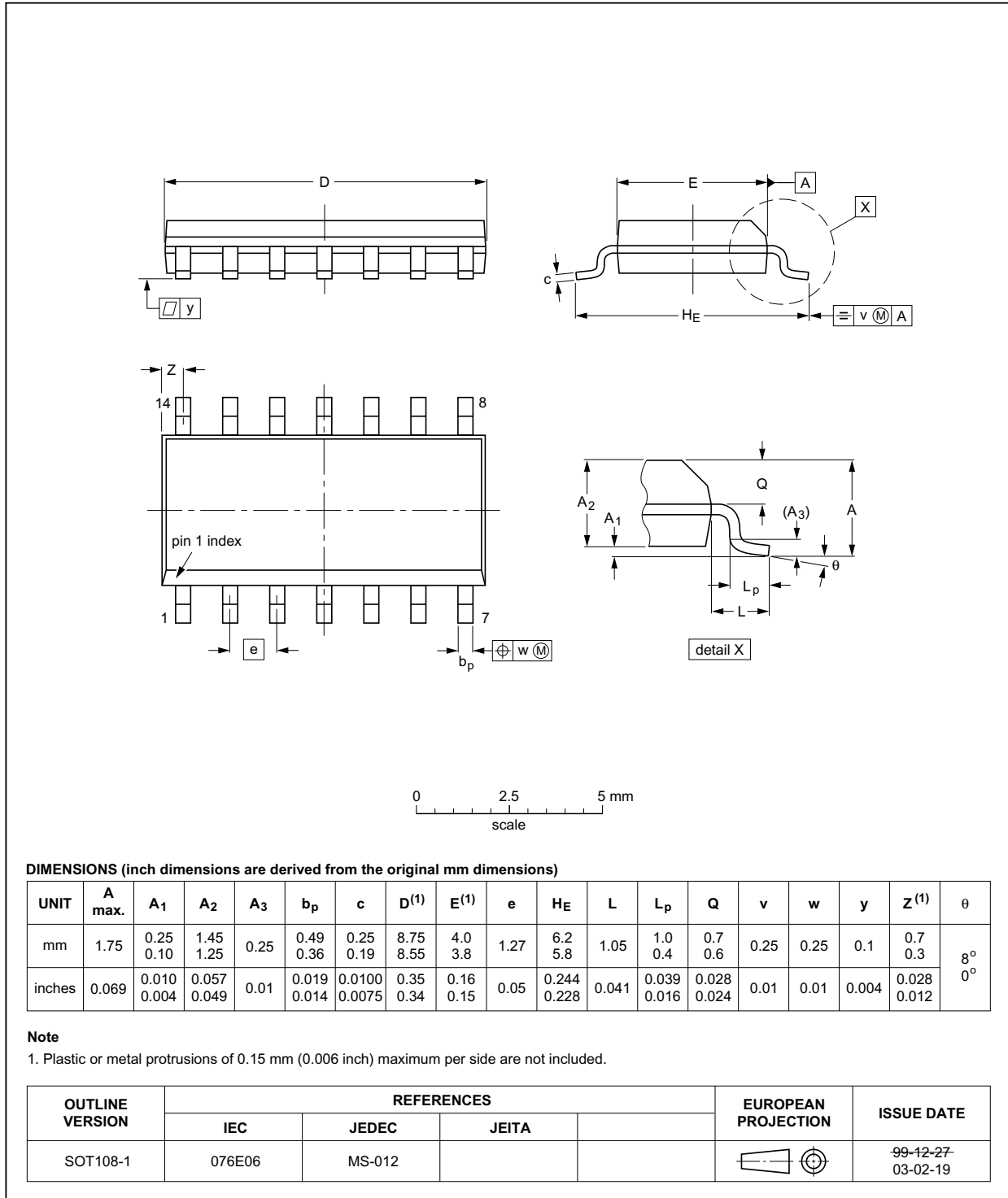


Quad 2-input AND gate

74HC08; 74HCT08

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



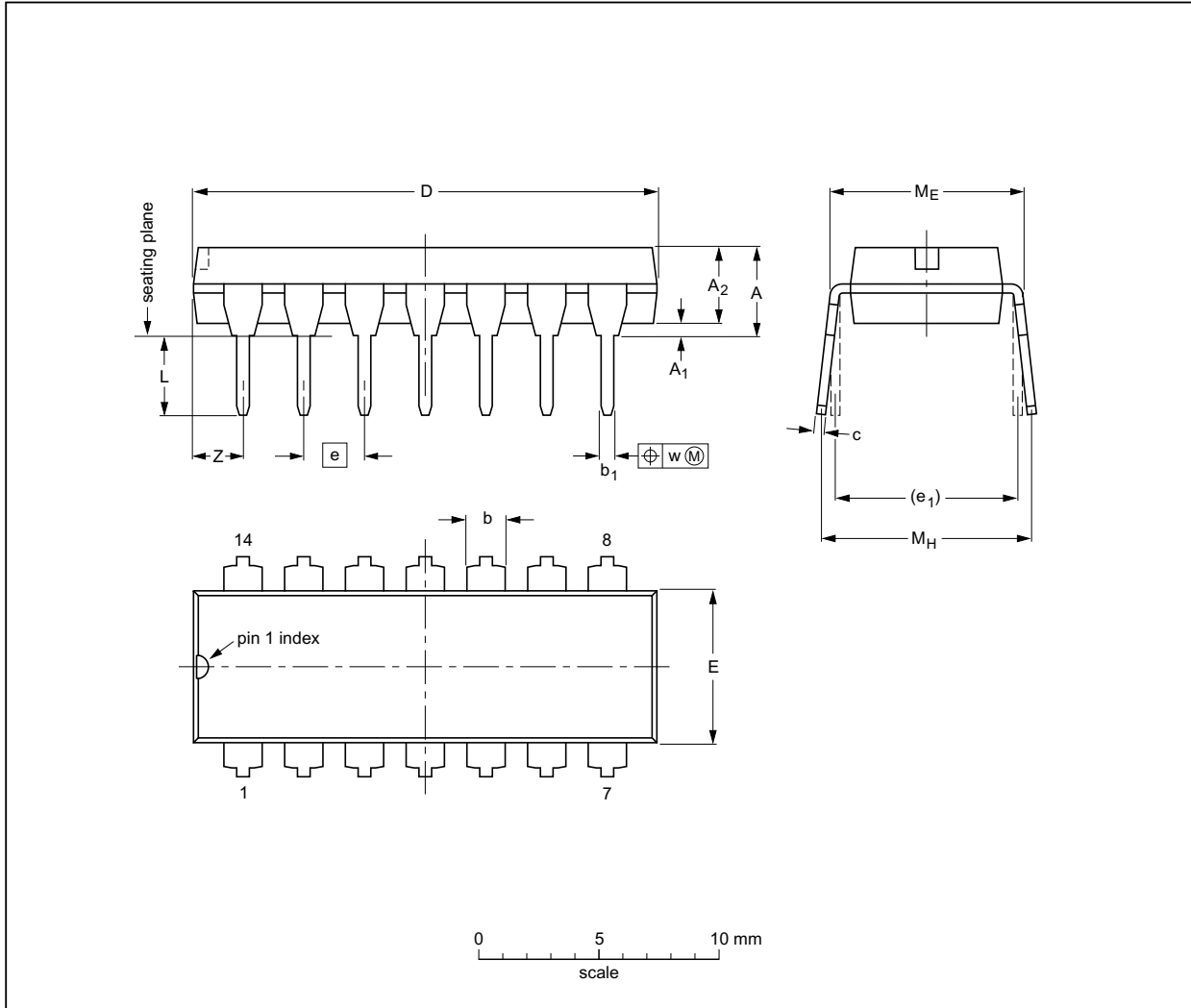
Quad 2-input AND gate

74HC08; 74HCT08

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

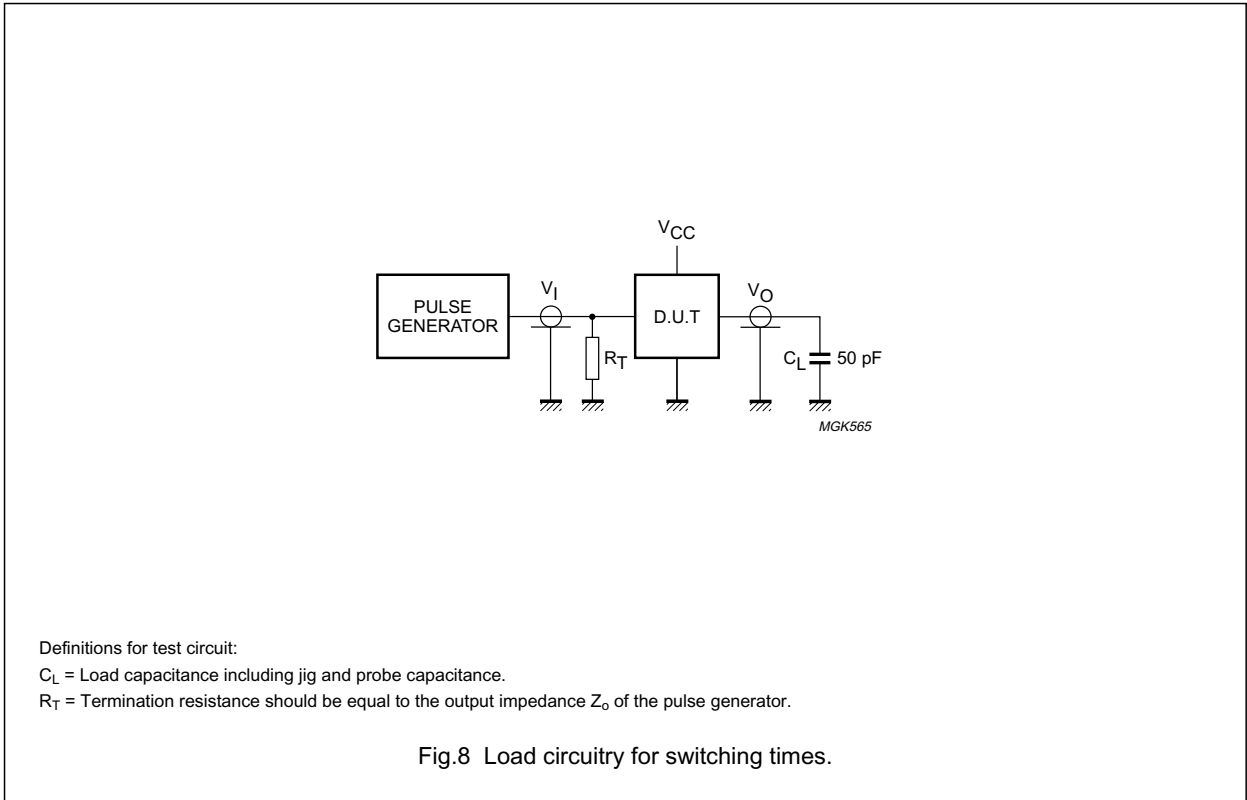
Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT27-1	050G04	MO-001	SC-501-14		99-12-27 03-02-13

Quad 2-input AND gate

74HC08; 74HCT08



Quad 2-input AND gate

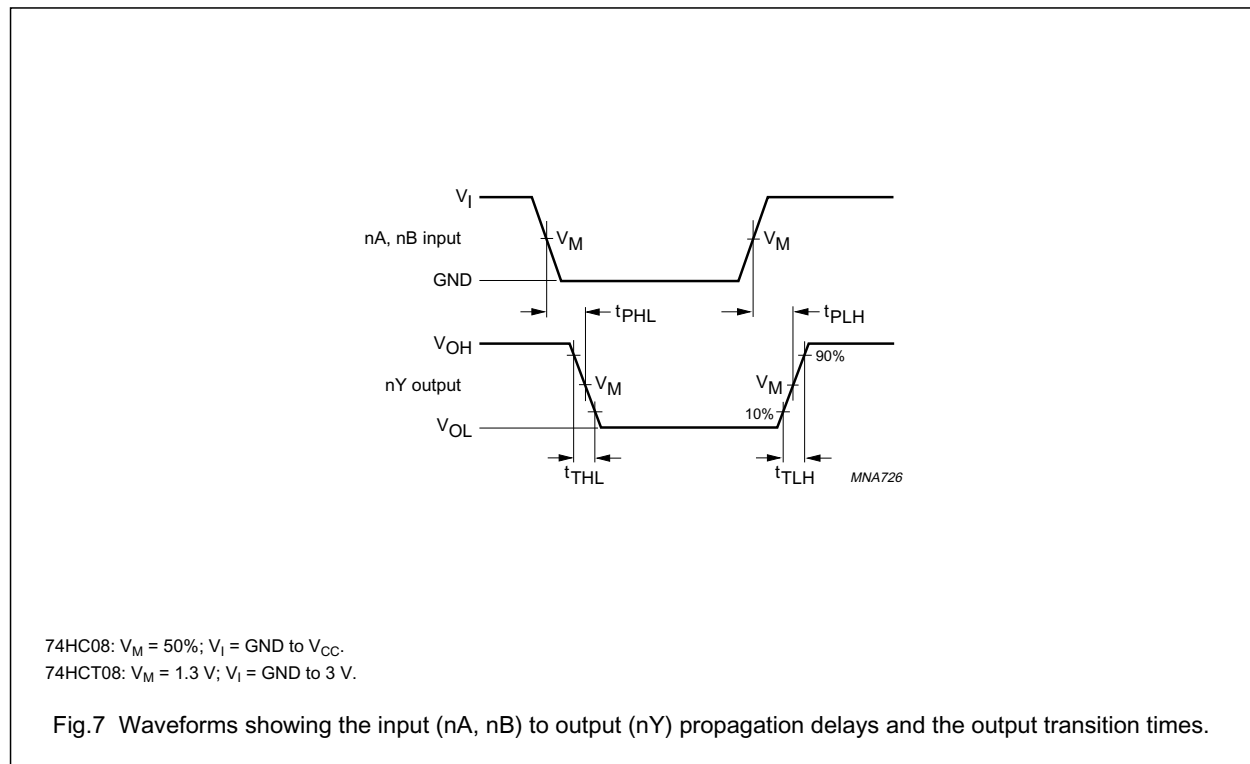
74HC08; 74HCT08

Family 74HCT08

GND = 0 V; $t_f = t_r = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
$T_{amb} = 25$ °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	4.5	–	14	24	ns
t_{THL}/t_{TLH}	output transition time	see Figs 7 and 8	4.5	–	7	15	ns
$T_{amb} = -40$ to $+85$ °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	4.5	–	–	30	ns
t_{THL}/t_{TLH}	output transition time	see Figs 7 and 8	4.5	–	–	19	ns
$T_{amb} = -40$ to $+125$ °C							
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	4.5	–	–	36	ns
t_{THL}/t_{TLH}	output transition time	see Figs 7 and 8	4.5	–	–	22	ns

AC WAVEFORMS



Quad 2-input AND gate

74HC08; 74HCT08

AC CHARACTERISTICS

Family 74HC08

GND = 0 V; $t_f = t_r = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = 25 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	2.0	–	25	90	ns
			4.5	–	9	18	ns
			6.0	–	7	15	ns
t _{THL} /t _{TLH}	output transition time	see Figs 7 and 8	2.0	–	19	75	ns
			4.5	–	7	15	ns
			6.0	–	6	13	ns
T_{amb} = –40 to +85 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	2.0	–	–	115	ns
			4.5	–	–	23	ns
			6.0	–	–	20	ns
t _{THL} /t _{TLH}	output transition time	see Figs 7 and 8	2.0	–	–	95	ns
			4.5	–	–	19	ns
			6.0	–	–	16	ns
T_{amb} = –40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Figs 7 and 8	2.0	–	–	135	ns
			4.5	–	–	27	ns
			6.0	–	–	23	ns
t _{THL} /t _{TLH}	output transition time	see Figs 7 and 8	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns

Quad 2-input AND gate

74HC08; 74HCT08

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -20 μA	4.5	4.4	–	–	V
		I _O = -4.0 mA	4.5	3.7	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 μA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	μA
I _{oz}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±10	μA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	40	μA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} - 2.1 V; I _O = 0	4.5 to 5.5	–	–	294	μA

Quad 2-input AND gate

74HC08; 74HCT08

Family 74HCT08

At recommended operating conditions; voltages are referenced to GND (ground = 0).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = 25 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –20 µA	4.5	4.4	4.5	–	V
		I _O = –4.0 mA	4.5	3.84	4.32	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±0.1	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±0.5	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	2	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	60	216	µA
T_{amb} = –40 to +85 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –20 µA	4.5	4.4	–	–	V
		I _O = –4.0 mA	4.5	3.84	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	20	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} – 2.1 V; I _O = 0	4.5 to 5.5	–	–	270	µA

Quad 2-input AND gate

74HC08; 74HCT08

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -20 µA	2.0	1.9	–	–	V
		I _O = -20 µA	4.5	4.4	–	–	V
		I _O = -4.0 mA	4.5	3.7	–	–	V
		I _O = -20 µA	6.0	5.9	–	–	V
		I _O = -5.2 mA	6.0	5.2	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	–	0.1	V
		I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
		I _O = 20 µA	6.0	–	–	0.1	V
		I _O = 5.2 mA	6.0	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±10.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	40	µA

Quad 2-input AND gate

74HC08; 74HCT08

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -20 µA	2.0	1.9	–	–	V
		I _O = -20 µA	4.5	4.4	–	–	V
		I _O = -4.0 mA	4.5	3.84	–	–	V
		I _O = -20 µA	6.0	5.9	–	–	V
		I _O = -5.2 mA	6.0	5.34	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	–	0.1	V
		I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.33	V
		I _O = 20 µA	6.0	–	–	0.1	V
		I _O = 5.2 mA	6.0	–	–	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	20	µA

Quad 2-input AND gate

74HC08; 74HCT08

DC CHARACTERISTICS

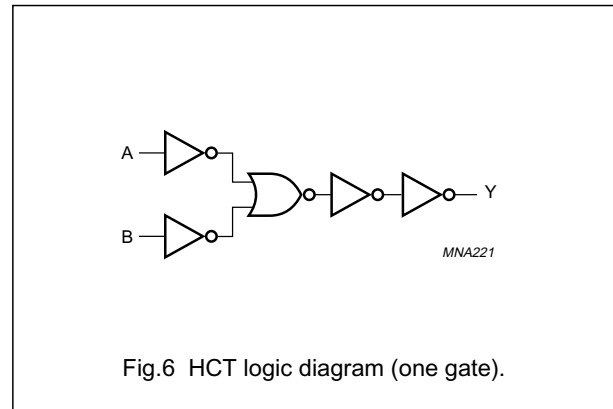
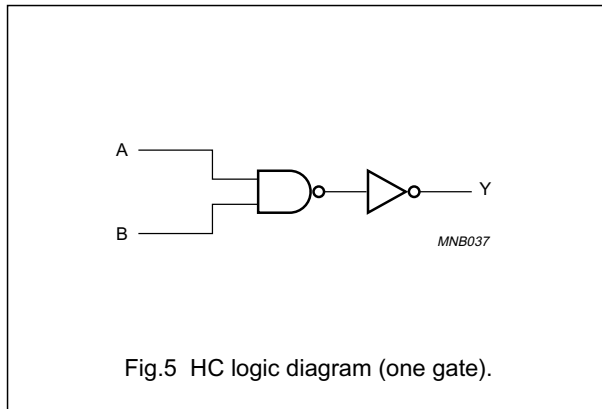
Family 74HC08

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = 25 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V _{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –20 µA	2.0	1.9	2.0	–	V
		I _O = –20 µA	4.5	4.4	4.5	–	V
		I _O = –4.0 mA	4.5	3.98	4.32	–	V
		I _O = –20 µA	6.0	5.9	6.0	–	V
		I _O = –5.2 mA	6.0	5.48	5.81	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	0	0.1	V
		I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.26	V
		I _O = 20 µA	6.0	–	0	0.1	V
		I _O = 5.2 mA	6.0	–	0.16	0.26	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	0.1	±0.1	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±0.5	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	2	µA

Quad 2-input AND gate

74HC08; 74HCT08



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC08			74HCT08			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

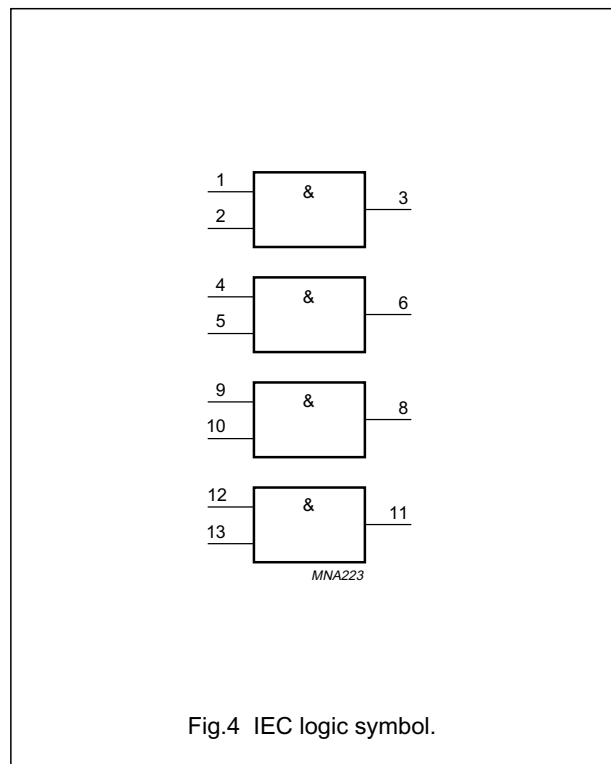
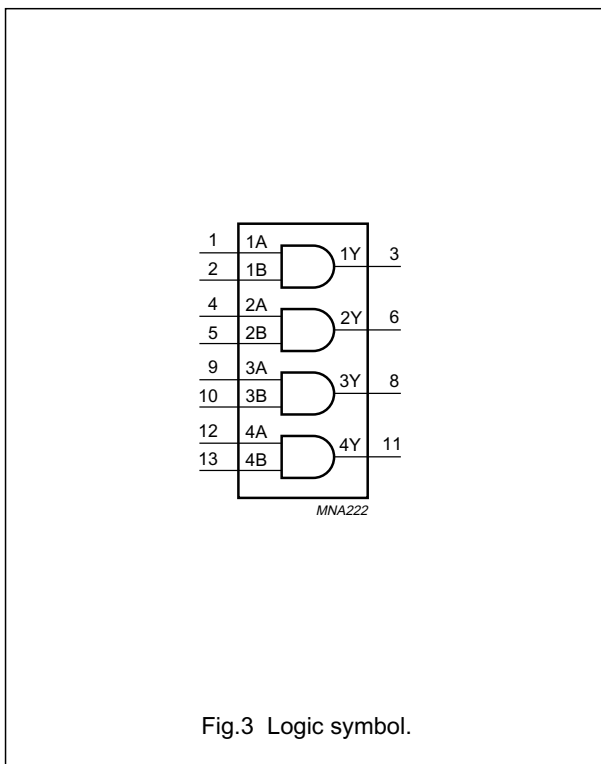
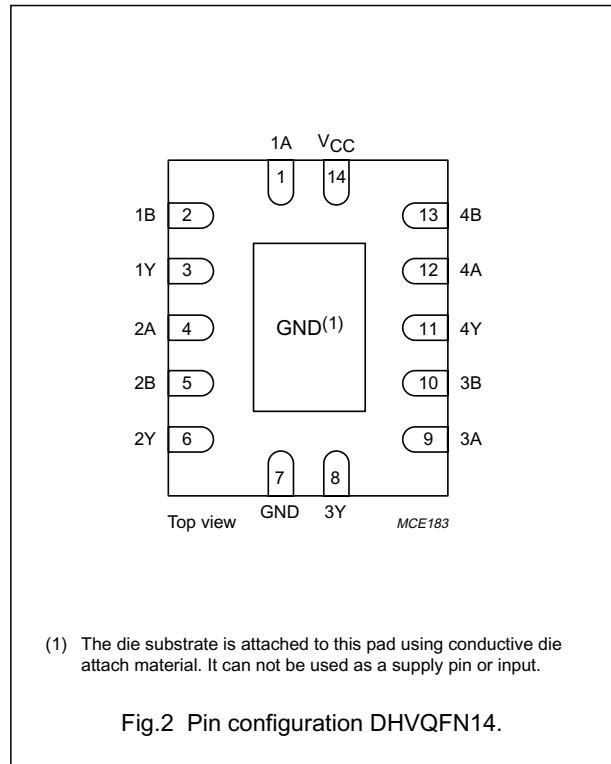
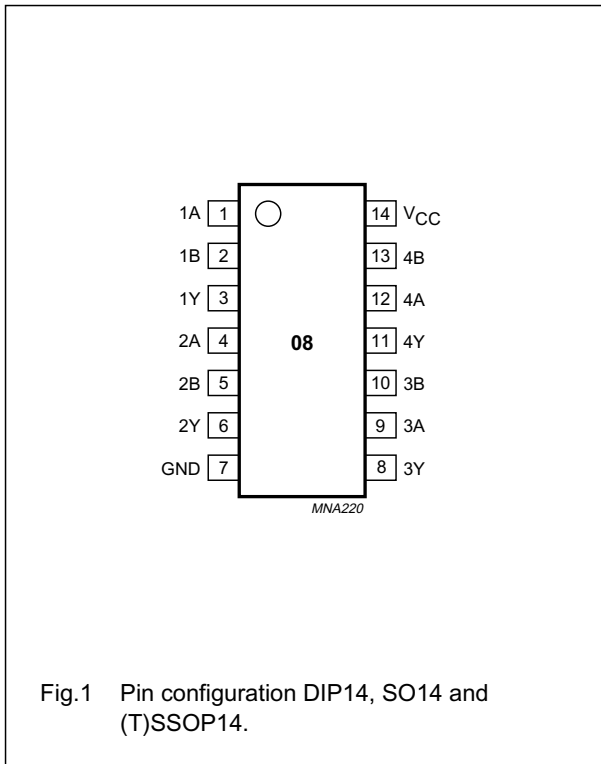
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	–	±20	mA
I_O	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation				
	DIP14 package	$T_{amb} = -40\text{ to }+125\text{ °C}$; note 1	–	750	mW
	other packages	$T_{amb} = -40\text{ to }+125\text{ °C}$; note 2	–	500	mW

Notes

- For DIP14 packages: above 70 °C derate linearly with 12 mW/K.
- For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

Quad 2-input AND gate

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Quad 2-input AND gate

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC08N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT08N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC08D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT08D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HC08DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT08DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC08PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT08PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC08BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT08BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V _{CC}	supply voltage

Quad 2-input AND gate

74HC08; 74HCT08

FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC08	74HCT08	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	$C_L = 15$ pF; $V_{CC} = 5$ V	7	11	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	10	20	pF

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

- For 74HC08: the condition is $V_I = \text{GND}$ to V_{CC} .

For 74HCT08: the condition is $V_I = \text{GND}$ to $V_{CC} - 1.5$ V.

FUNCTION TABLE

INPUT		OUTPUT
nA	nB	nY
L	L	L
L	H	L
H	L	L
H	H	H

Note

- H = HIGH voltage level;
L = LOW voltage level.

DATA SHEET

74HC08; 74HCT08 Quad 2-input AND gate

Product specification
Supersedes data of 1990 Dec 01

2003 Jul 25