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Quad 2-input NAND gate

74HC00; 74HCT00

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device.

These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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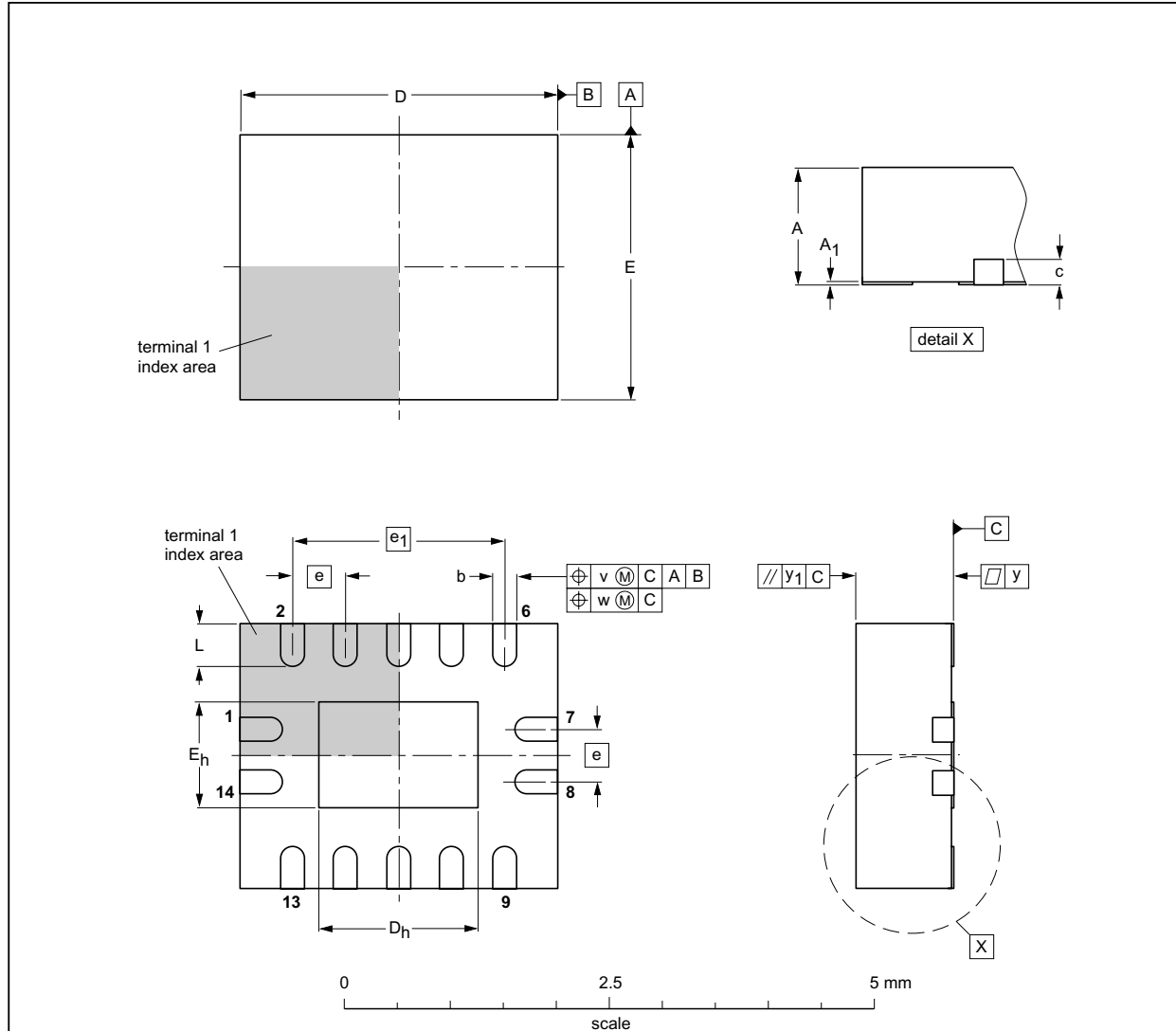
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Quad 2-input NAND gate

74HC00; 74HCT00

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



DIMENSIONS (mm are the original dimensions)

UNIT	A ⁽¹⁾ max.	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	L	v	w	y	y ₁
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.65 1.35	2.6 2.4	1.15 0.85	0.5	2	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

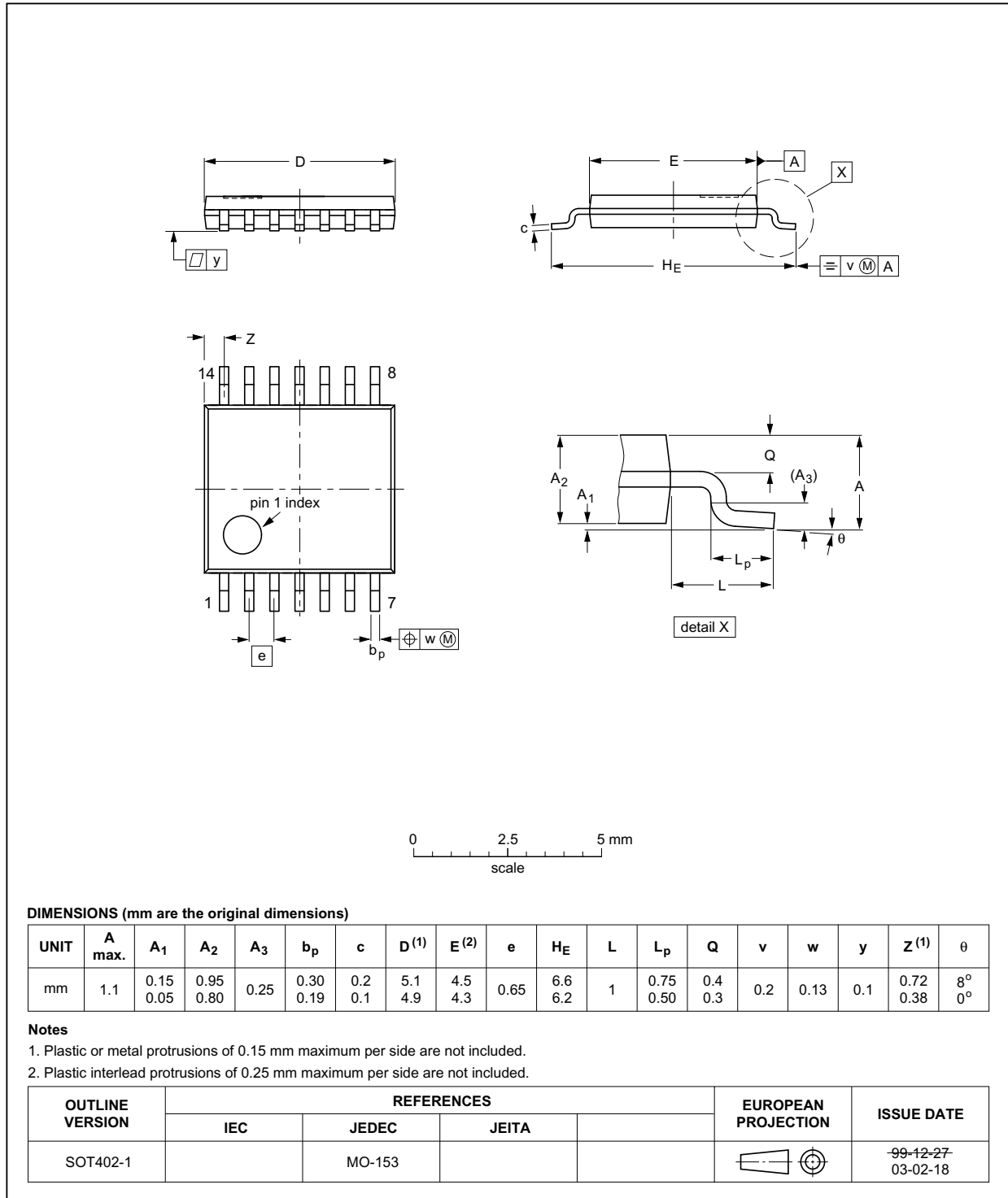
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT762-1	---	MO-241	---			02-10-17 03-01-27

Quad 2-input NAND gate

74HC00; 74HCT00

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

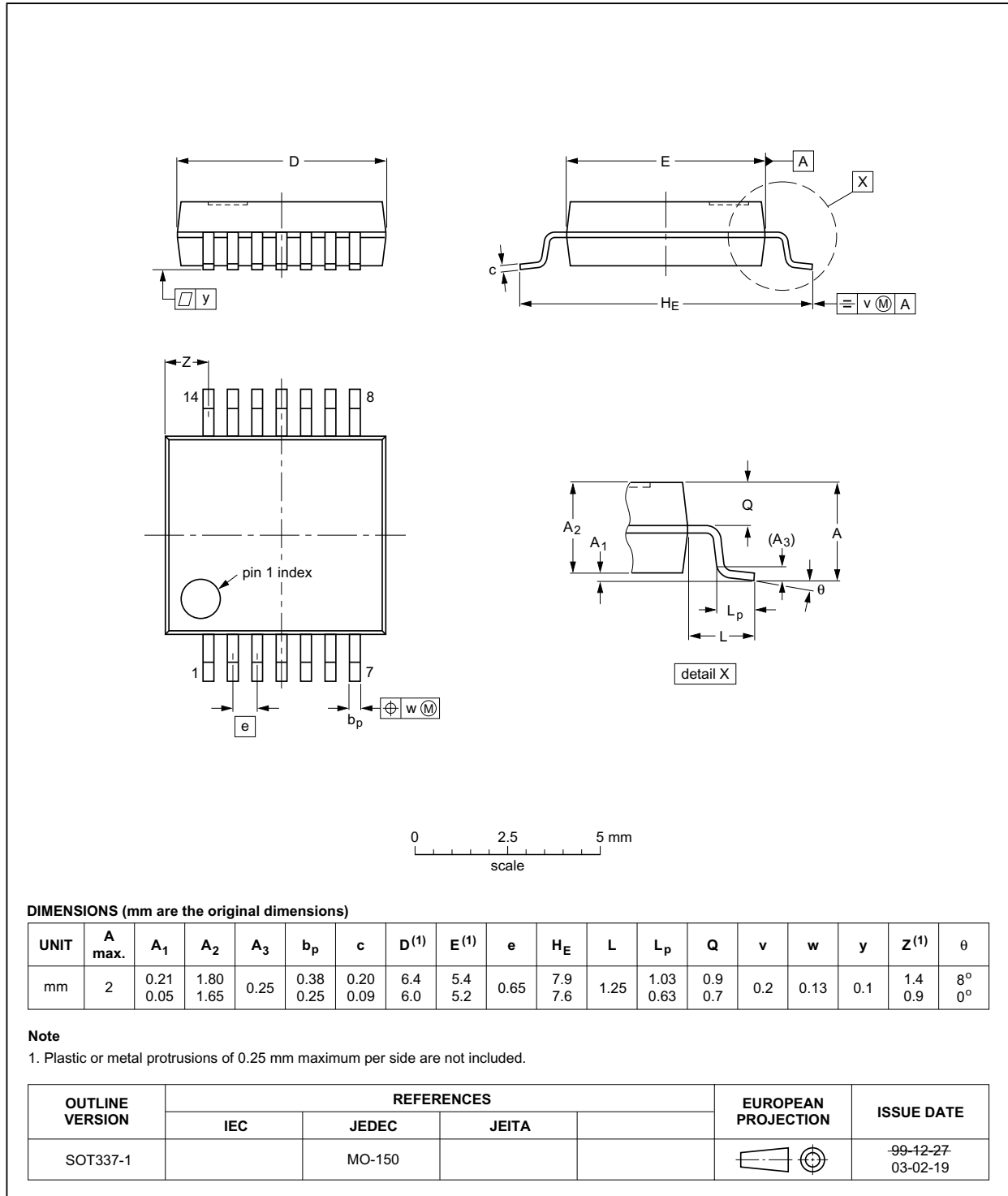


Quad 2-input NAND gate

74HC00; 74HCT00

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

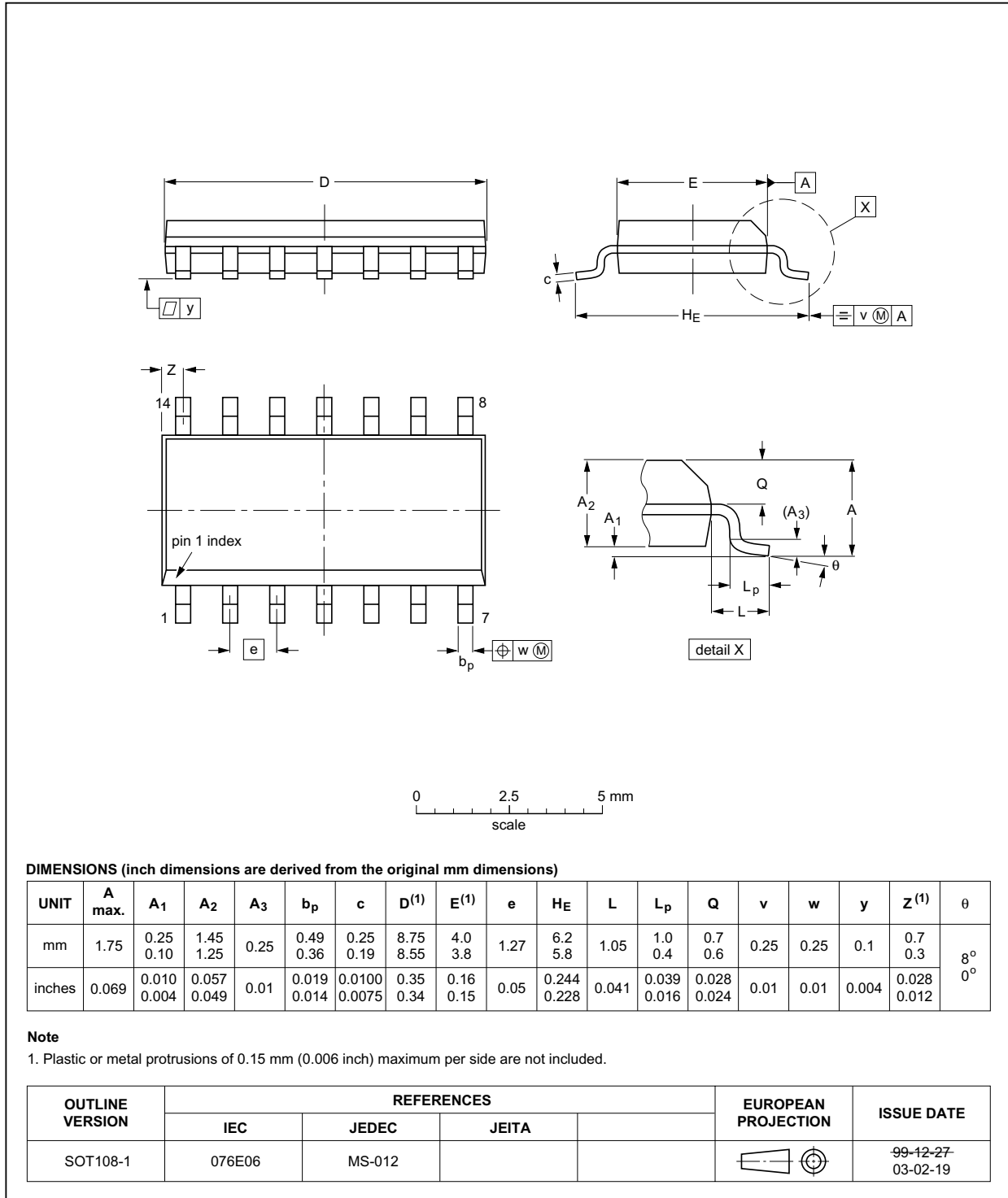


Quad 2-input NAND gate

74HC00; 74HCT00

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



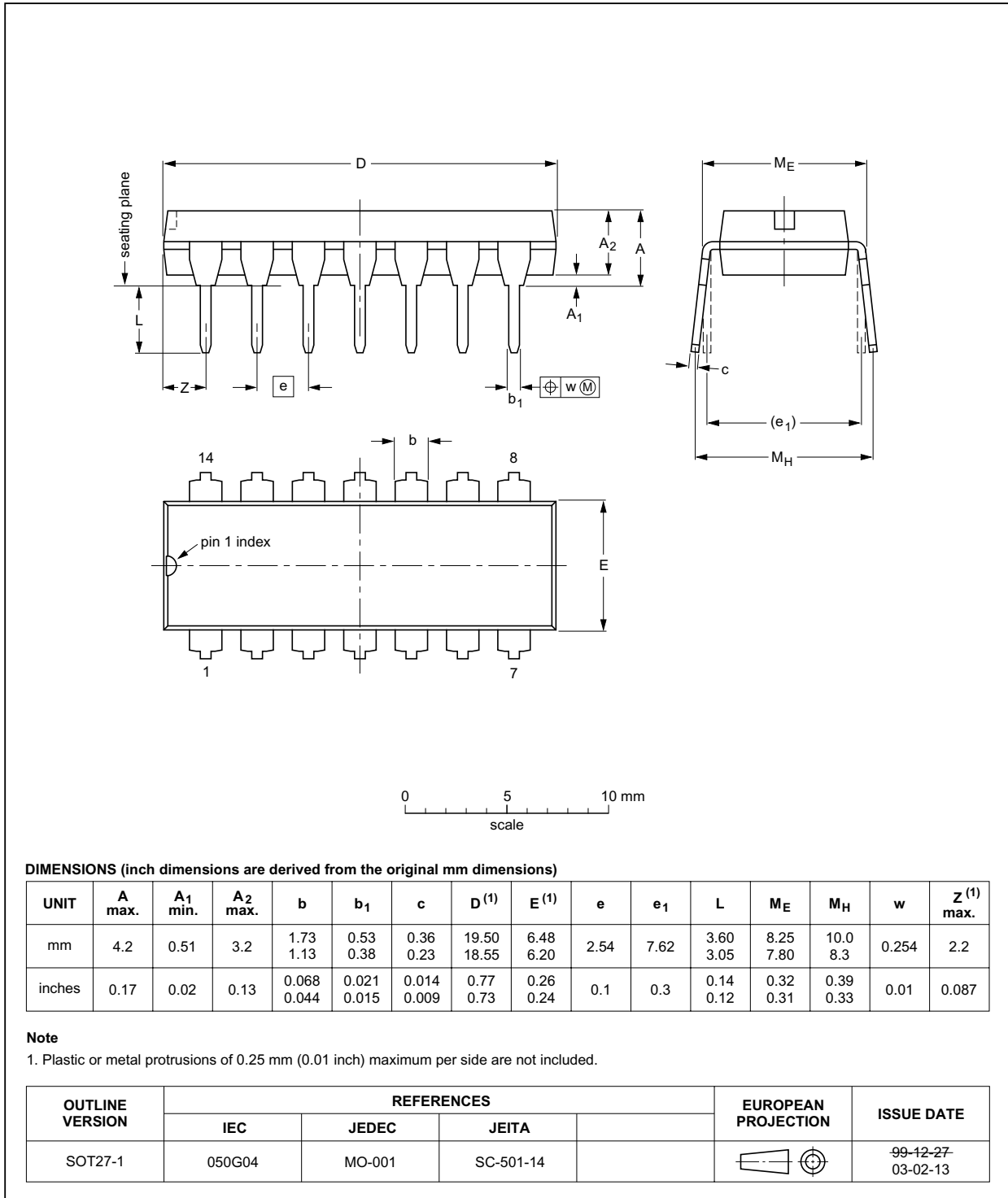
Quad 2-input NAND gate

74HC00; 74HCT00

PACKAGE OUTLINES

DIP14: plastic dual in-line package; 14 leads (300 mil)

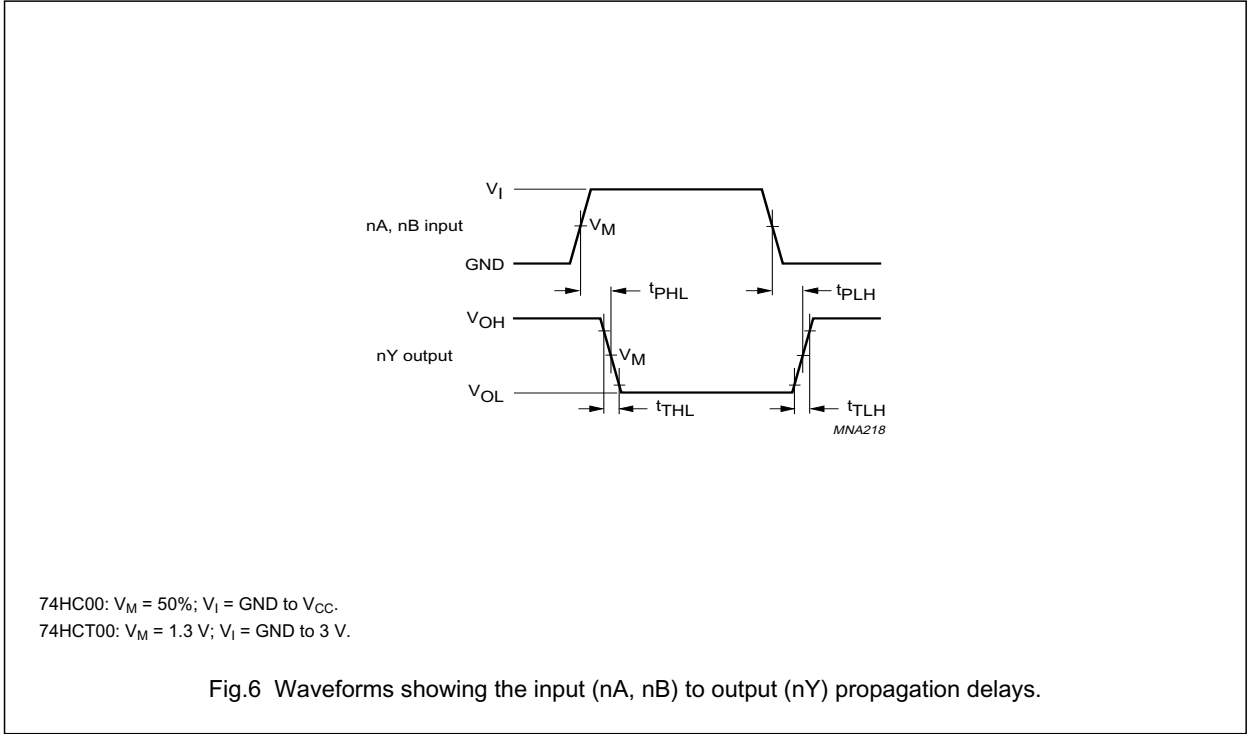
SOT27-1



Quad 2-input NAND gate

74HC00; 74HCT00

AC WAVEFORMS



Quad 2-input NAND gate

74HC00; 74HCT00

AC CHARACTERISTICS

Type 74HC00

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Fig.6	2.0	–	25	115	ns
		see Fig.6	4.5	–	9	23	ns
		see Fig.6	6.0	–	7	20	ns
t _{THL} /t _{TLH}	output transition time		2.0	–	19	95	ns
			4.5	–	7	19	ns
			6.0	–	6	16	ns
T_{amb} = -40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Fig.6	2.0	–	–	135	ns
		see Fig.6	4.5	–	–	27	ns
		see Fig.6	6.0	–	–	23	ns
t _{THL} /t _{TLH}	output transition time		2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Type 74HCT00

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Fig.6	4.5	–	12	24	ns
t _{THL} /t _{TLH}	output transition time		4.5	–	–	29	ns
T_{amb} = -40 to +125 °C							
t _{PHL} /t _{PLH}	propagation delay nA, nB to nY	see Fig.6	4.5	–	–	29	ns
t _{THL} /t _{TLH}	output transition time		4.5	–	–	22	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

Quad 2-input NAND gate

74HC00; 74HCT00

Type 74HCT00

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -20 µA	4.5	4.4	4.5	–	V
		I _O = -4.0 mA	4.5	3.84	4.32	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	20	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} - 2.1 V; I _O = 0	4.5 to 5.5	–	150	675	µA
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V _{IL}	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -20 µA	4.5	4.4	–	–	V
		I _O = -4.0 mA	4.5	3.7	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	5.5	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; I _O = 0	5.5	–	–	±10	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	5.5	–	–	40	µA
ΔI _{CC}	additional supply current per input	V _I = V _{CC} - 2.1 V; I _O = 0	4.5 to 5.5	–	–	735	µA

Note1. All typical values are measured at T_{amb} = 25 °C.

Quad 2-input NAND gate

74HC00; 74HCT00

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +125 °C							
V _{IH}	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V _{IL}	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = -20 µA	2.0	1.9	–	–	V
		I _O = -20 µA	4.5	4.4	–	–	V
		I _O = -20 µA	6.0	5.9	–	–	V
		I _O = -4.0 mA	4.5	3.7	–	–	V
		I _O = -5.2 mA	6.0	5.2	–	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	–	0.1	V
		I _O = 20 µA	4.5	–	–	0.1	V
		I _O = 20 µA	6.0	–	–	0.1	V
		I _O = 4.0 mA	4.5	–	–	0.4	V
		I _O = 5.2 mA	6.0	–	–	0.4	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±10.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	40	µA

Note

1. All typical values are measured at T_{amb} = 25 °C.

Quad 2-input NAND gate

74HC00; 74HCT00

DC CHARACTERISTICS

Type 74HC00

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V _{CC} (V)				
T_{amb} = -40 to +85 °C; note 1							
V _{IH}	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V _{IL}	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} I _O = –20 µA	2.0	1.9	2.0	–	V
		I _O = –20 µA	4.5	4.4	4.5	–	V
		I _O = –20 µA	6.0	5.9	6.0	–	V
		I _O = –4.0 mA	4.5	3.84	4.32	–	V
		I _O = –5.2 mA	6.0	5.34	5.81	–	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} I _O = 20 µA	2.0	–	0	0.1	V
		I _O = 20 µA	4.5	–	0	0.1	V
		I _O = 20 µA	6.0	–	0	0.1	V
		I _O = 4.0 mA	4.5	–	0.15	0.33	V
		I _O = 5.2 mA	6.0	–	0.16	0.33	V
I _{LI}	input leakage current	V _I = V _{CC} or GND	6.0	–	–	±1.0	µA
I _{OZ}	3-state output OFF current	V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND	6.0	–	–	±5.0	µA
I _{CC}	quiescent supply current	V _I = V _{CC} or GND; I _O = 0	6.0	–	–	20	µA

Quad 2-input NAND gate

74HC00; 74HCT00

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC00			74HCT00			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	$V_{CC} = 2.0\text{ V}$	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5\text{ V}$	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0\text{ V}$	–	–	400	–	–	–	ns

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

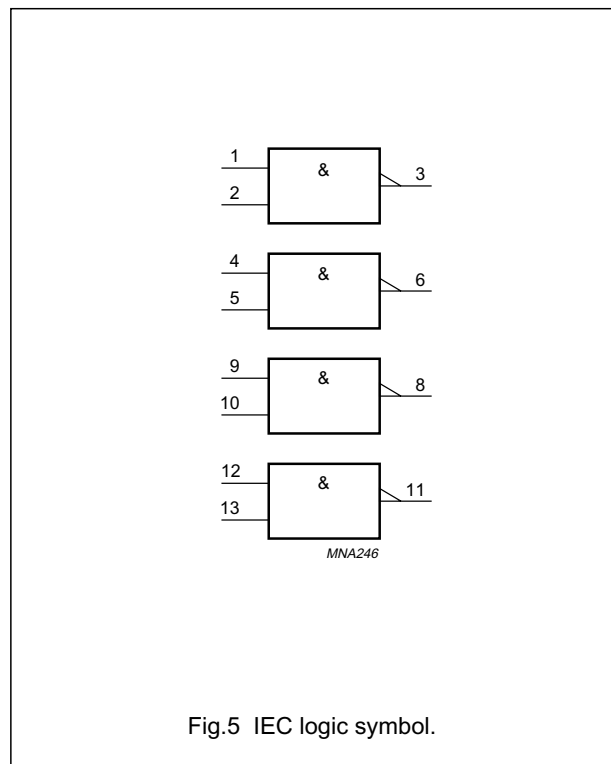
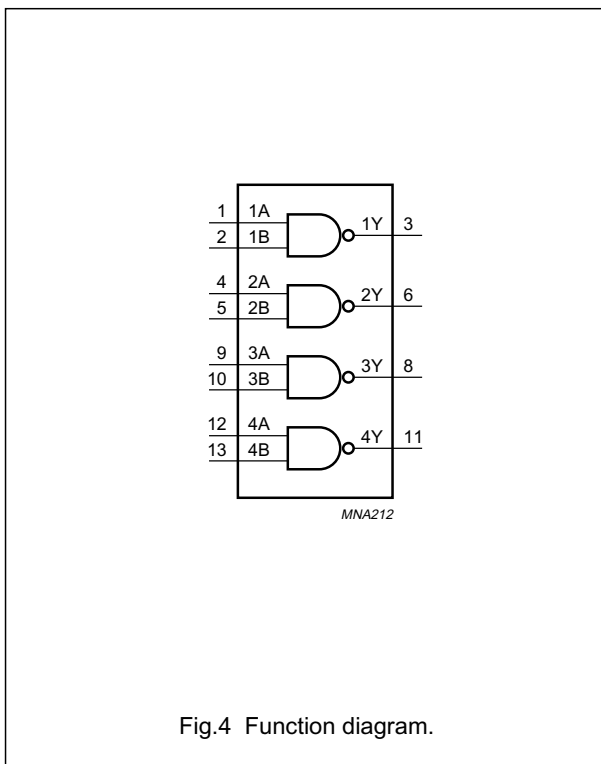
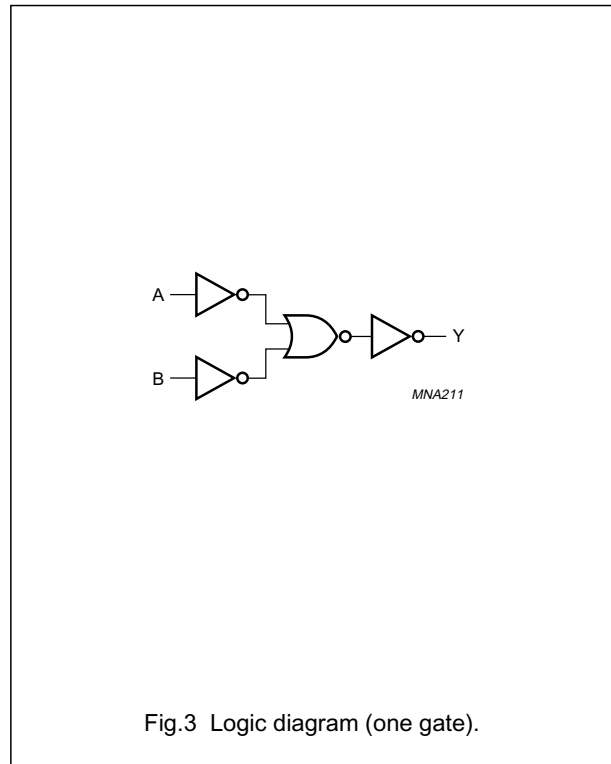
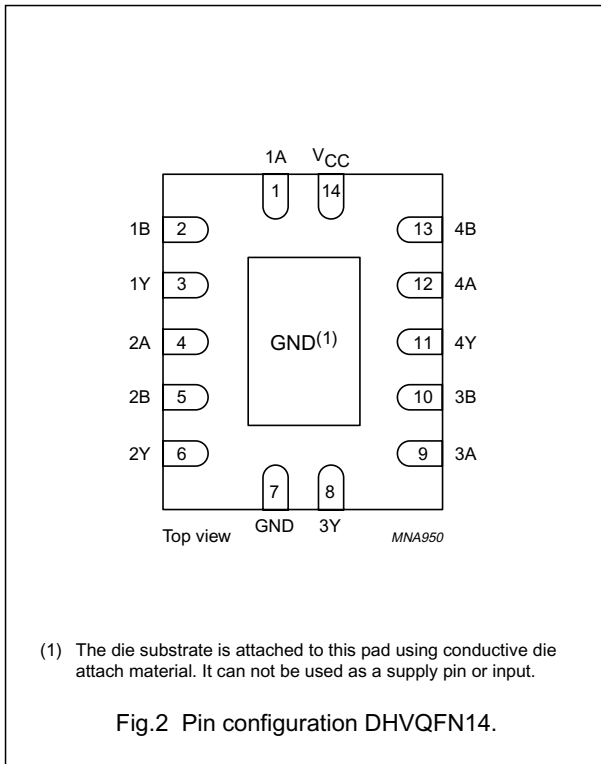
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+7.0	V
I_{IK}	input diode current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	–	±20	mA
I_{OK}	output diode current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	–	±20	mA
I_O	output source or sink current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	–	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±50	mA
T_{stg}	storage temperature		–65	+150	°C
P_{tot}	power dissipation	$T_{amb} = -40\text{ to }+125\text{ °C}$; note 1	–	500	mW

Note

- For DIP14 packages: above 70 °C derate linearly with 12 mW/K.
For SO14 packages: above 70 °C derate linearly with 8 mW/K.
For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.
For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

Quad 2-input NAND gate

74HC00; 74HCT00



Quad 2-input NAND gate

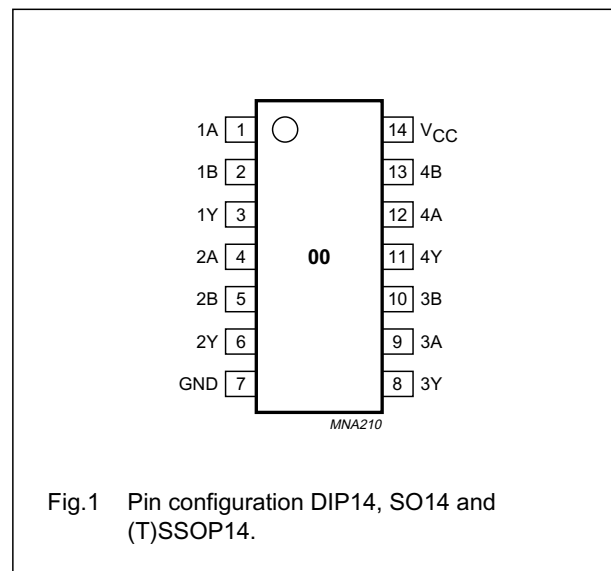
74HC00; 74HCT00

ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74HC00N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HCT00N	-40 to +125 °C	14	DIP14	plastic	SOT27-1
74HC00D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HCT00D	-40 to +125 °C	14	SO14	plastic	SOT108-1
74HC00DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HCT00DB	-40 to +125 °C	14	SSOP14	plastic	SOT337-1
74HC00PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HCT00PW	-40 to +125 °C	14	TSSOP14	plastic	SOT402-1
74HC00BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1
74HCT00BQ	-40 to +125 °C	14	DHVQFN14	plastic	SOT762-1

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1B	data input
3	1Y	data output
4	2A	data input
5	2B	data input
6	2Y	data output
7	GND	ground (0 V)
8	3Y	data output
9	3A	data input
10	3B	data input
11	4Y	data output
12	4A	data input
13	4B	data input
14	V _{CC}	supply voltage



Quad 2-input NAND gate

74HC00; 74HCT00

FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection:
HBM EIA/JESD22-A114-A exceeds 2000 V
MM EIA/JESD22-A115-A exceeds 200 V
- Specified from -40 to $+85$ °C and -40 to $+125$ °C.

DESCRIPTION

The 74HC00/74HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC00/74HCT00 provide the 2-input NAND function.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25$ °C; $t_r = t_f = 6$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			74HC00	74HCT00	
t_{PHL}/t_{PLH}	propagation delay nA, nB to nY	$C_L = 15$ pF; $V_{CC} = 5$ V	7	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	22	22	pF

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in Volts;

N = total load switching outputs;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

- For 74HC00 the condition is $V_I = \text{GND to } V_{CC}$.

For 74HCT00 the condition is $V_I = \text{GND to } V_{CC} - 1.5$ V.

FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nB	nY
L	L	H
L	H	H
H	L	H
H	H	L

Note

- H = HIGH voltage level;
L = LOW voltage level.

DATA SHEET

74HC00; 74HCT00 Quad 2-input NAND gate

Product specification
Supersedes data of 1997 Aug 26

2003 Jun 30